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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,359	04/20/2004	Richard Carl Phelps	0120-029	2610

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,359	PHELPS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,592,631 to Kelly et al. ("Kelly").

3. In reference to Claim 1, Kelly discloses an apparatus for use in a computer system comprising: a bus architecture (See Figure 2 Number 204); a plurality of modules connected to the bus architecture (See Figure 2 Numbers 203, 218, 219, and 220); and a centralized bus arbiter (See Figure 3 Number 300) comprising: a first arbiter means for controlling initiating transactions on the bus architecture (See Figure 1 and Column 2 Line 60 – Column 3 Line 2); and a second arbiter means for controlling return transactions on the bus architecture (See Figure 1 and Column 3

Lines 3-13); the first and second arbiter means operating independently of each other (See Column 2 Lines 40-43).

4. In reference to Claim 3, Kelly discloses the limitations as applied to Claim 1 above. Kelly further discloses a computer system comprising the apparatus (See Column 1 Lines 7-8).

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,012,118 to Jayakumar et al. ("Jayakumar").

6. In reference to Claim 1, Jayakumar discloses an apparatus for use in a computer system comprising: a bus architecture (See Figure 2); a plurality of modules connected to the bus architecture (See Figure 2); and a centralized bus arbiter (See Column 7 Lines 46-49) comprising: a first arbiter means for controlling initiating transactions on the bus architecture (See Figure 3 Number 300); and a second arbiter means for controlling return transactions on the bus architecture (See Figure 3 Number 308); the first and second arbiter means operating independently of each other (See Column 6 Lines 18-23).

7. In reference to Claim 3, Jayakumar discloses the limitations as applied to Claim 1 above. Jayakumar further discloses a computer system comprising the apparatus (See Column 1 Lines 11-14).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly as applied to Claim 1 above, and further in view of US Patent Number 5,060,145 to Scheuneman et al. ("Scheuneman").

10. In reference to Claim 2, Kelly discloses the limitations as applied to Claim 1 above. Kelly further discloses that the bus architecture has separate data (See Figure 2 Number 205) and transaction (See Figure 2 Number 206) buses, and wherein the first arbiter means controls writes and transactions (See Column 2 Line 60 – Column 3 Line 2 and Column 8 Lines 61-64) and the second arbiter means controls return transactions on the bus (See Column 3 Lines 3-13). Kelly does not disclose that the data bus is composed of separate read and write buses. Scheuneman teaches that it is well known to use separate read (See Figure 1 Number 16) and write (See Figure 1 Number 17) buses.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to separate the single data bus of Kelly into separate read and write buses as taught by Scheuneman, resulting in the invention of Claim 2, in order to allow read and write requests to be operated in parallel, and thus improve the efficiency and bandwidth of the system by reducing bus contention (See Column 1 Lines 58-61 of Scheuneman).

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly as applied to Claim 1 above, and further in view of US Patent Number 5,838,603 to Mori et al. ("Mori").

12. In reference to Claim 4, Kelly discloses the limitations as applied to Claim 1 above. Kelly does not disclose an integrated circuit comprising the apparatus. Mori teaches that it is well known to construct computer systems on a single integrated circuit (See Column 8 Lines 29-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the computer system of Kelly as a system-on-chip as taught by Mori, resulting in the invention of Claim 4, in order to improve various characteristics of the system such as the operational speed, and reduce the production cost of the system (See Column 8 Lines 31-34 of Mori).

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly as applied to Claim 1 above, and further in view of US Patent Number 5,046,023 to Katsura et al. ("Katsura").

14. In reference to Claim 5, Kelly discloses the limitations as applied to Claim 1 above. Kelly does not disclose a graphics processing system comprising the apparatus. Katsura teaches a graphics processing system having a plurality of modules arbitrating for access to a bus (See Column 10 Lines 31-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the graphics processing system of Katsura with the bus system and arbitration of Kelly, resulting in the invention of Claim 5, in order to improve the bus-memory throughput by allowing other bus traffic to use the system bus during the actual memory access by allowing the address bus and data bus to have different masters at the same time (See Column 2 Lines 8-11 and 56-57 and Column 3 Lines 23-25 of Kelly).

15. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly as applied to Claim 1 above, and further in view of US Patent Number 5,016,876 to Loffredo ("Loffredo").

16. In reference to Claim 6, Kelly discloses the limitations as applied to Claim 1 above. Kelly does not disclose a games console comprising the apparatus. Loffredo

teaches a games console having a plurality of modules arbitrating for access to a bus (See Column 22 Line 62 – Column 23 Line 41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the games console of Loffredo with the bus system and arbitration of Kelly, resulting in the invention of Claim 6, in order to improve the bus-memory throughput by allowing other bus traffic to use the system bus during the actual memory access by allowing the address bus and data bus to have different masters at the same time (See Column 2 Lines 8-11 and 56-57 and Column 3 Lines 23-25 of Kelly).

17. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jayakumar as applied to Claim 1 above, and further in view of Scheuneman.

18. In reference to Claim 2, Jayakumar discloses the limitations as applied to Claim 1 above. Jayakumar further discloses that the bus architecture has separate data (See Column 4 Lines 44-46) and transaction (See Column 4 Lines 37-44) buses, and wherein the first arbiter means controls writes and transactions (See Figure 3 Number 301 and Column 5 Lines 3-5) and the second arbiter means controls return transactions on the bus (See Figure 3 Number 308 and Column 5 Lines 5-7). Jayakumar does not disclose that the data bus is composed of separate read and write buses. Scheuneman teaches that it is well known to use separate read (See Figure 1 Number 16) and write (See Figure 1 Number 17) buses.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to separate the single data bus of Jayakumar into separate read and write buses as taught by Scheuneman, resulting in the invention of Claim 2, in order to allow read and write requests to be operated in parallel, and thus improve the efficiency and bandwidth of the system by reducing bus contention (See Column 1 Lines 58-61 of Scheuneman).

19. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jayakumar as applied to Claim 1 above, and further in view of Mori.

20. In reference to Claim 4, Jayakumar discloses the limitations as applied to Claim 1 above. Jayakumar does not disclose an integrated circuit comprising the apparatus. Mori teaches that it is well known to construct computer systems on a single integrated circuit (See Column 8 Lines 29-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the computer system of Jayakumar as a system-on-chip as taught by Mori, resulting in the invention of Claim 4, in order to improve various characteristics of the system such as the operational speed, and reduce the production cost of the system (See Column 8 Lines 31-34 of Mori).

21. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jayakumar as applied to Claim 1 above, and further in view of Katsura.

22. In reference to Claim 5, Jayakumar discloses the limitations as applied to Claim 1 above. Jayakumar does not disclose a graphics processing system comprising the apparatus. Katsura teaches a graphics processing system having a plurality of modules arbitrating for access to a bus (See Column 10 Lines 31-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the graphics processing system of Katsura with the bus system and arbitration of Jayakumar, resulting in the invention of Claim 5, in order improve the latency, bandwidth, and scalability of the system (See Column 3 Lines 1-5 of Jayakumar).

23. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jayakumar as applied to Claim 1 above, and further in view of Loffredo.

24. In reference to Claim 6, Jayakumar discloses the limitations as applied to Claim 1 above. Jayakumar does not disclose a games console comprising the apparatus. Loffredo teaches a games console having a plurality of modules arbitrating for access to a bus (See Column 22 Line 62 – Column 23 Line 41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the games console of Loffredo with the bus system and arbitration of Jayakumar, resulting in the invention of Claim 6, in order improve the

latency, bandwidth, and scalability of the system (See Column 3 Lines 1-5 of Jayakumar).

Response to Arguments

25. Applicant's arguments with respect to Claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC

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